

Fig. 1A
(Prior Art)

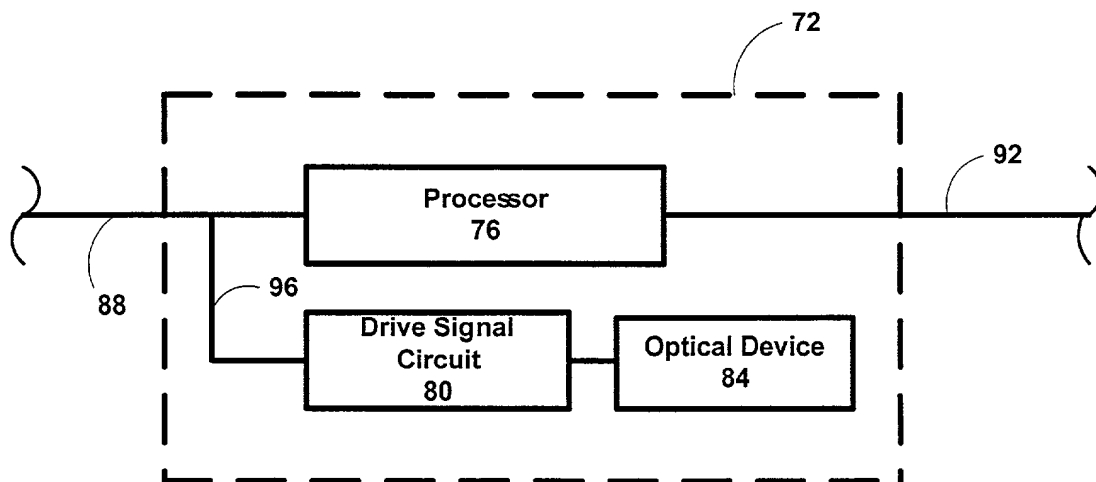


Fig. 4

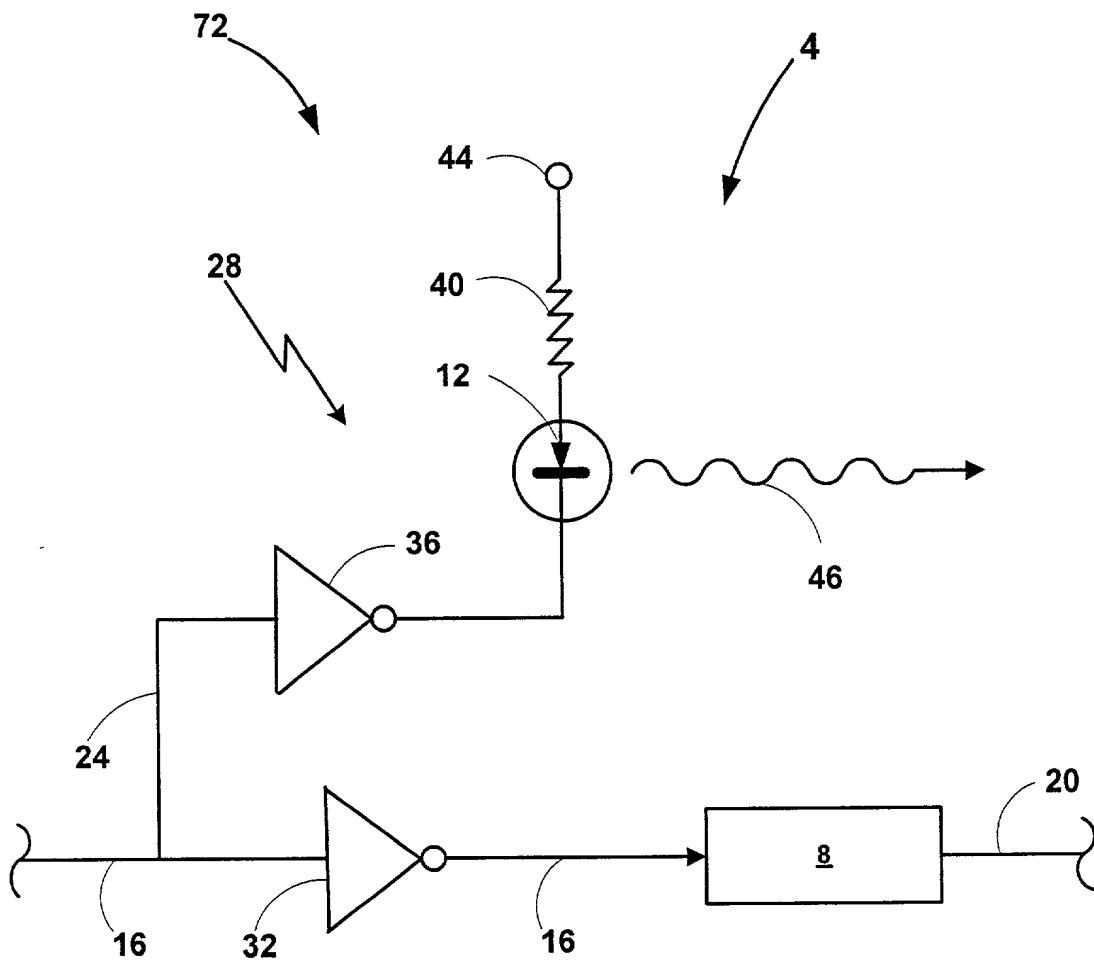
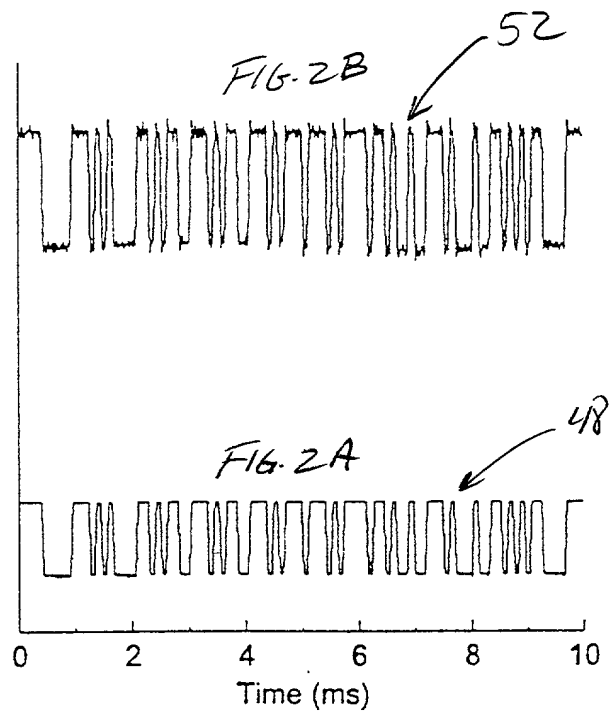


Fig. 1B
(Prior Art)



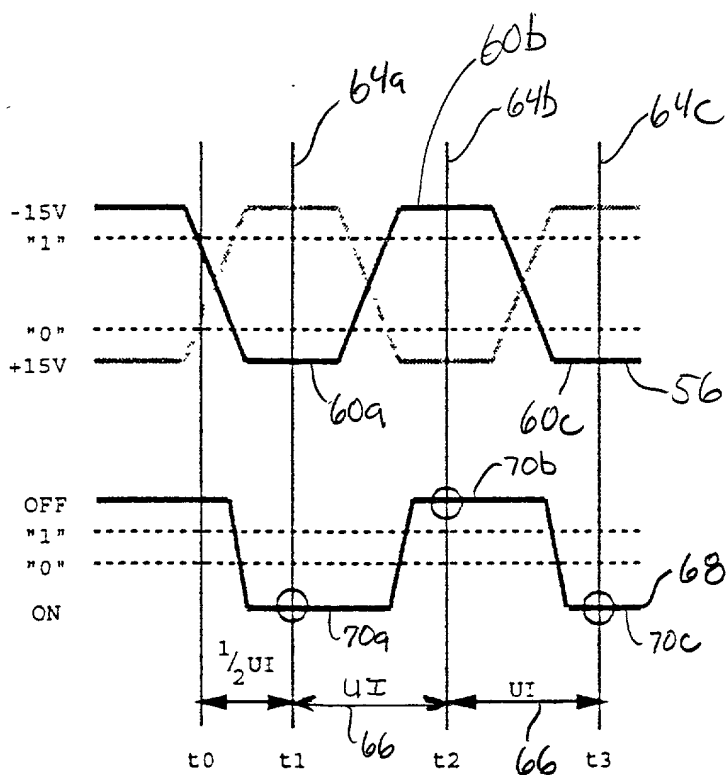


FIG. 3

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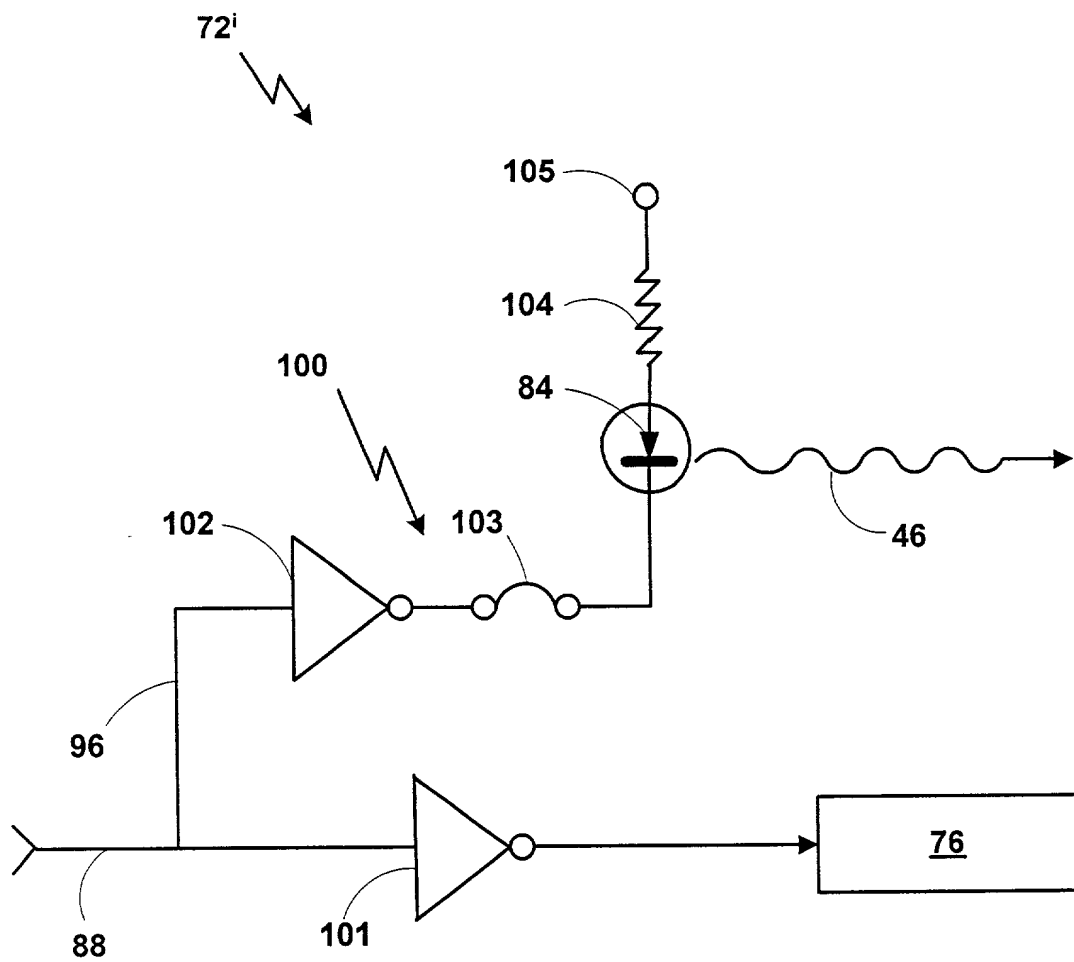


Fig. 5

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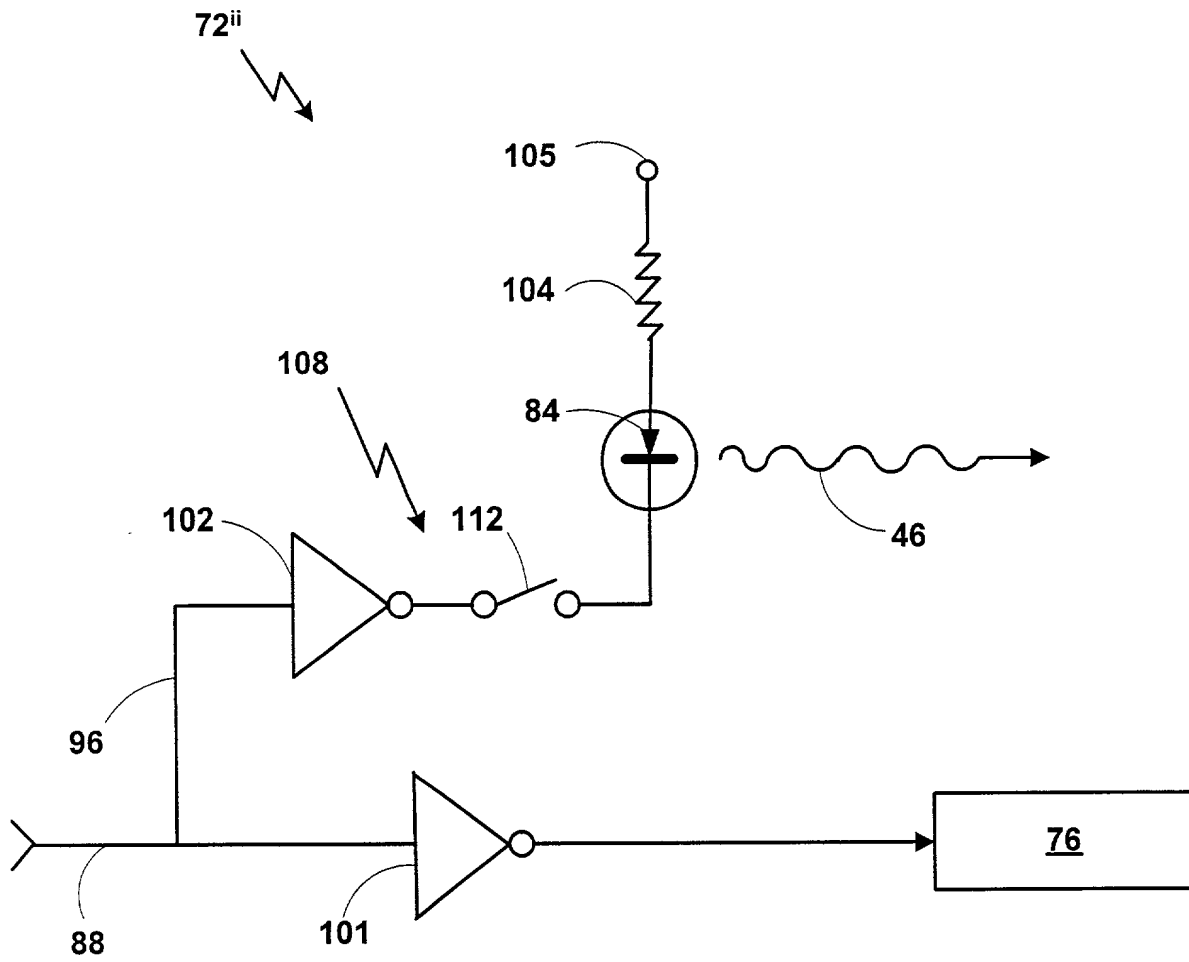


Fig. 6

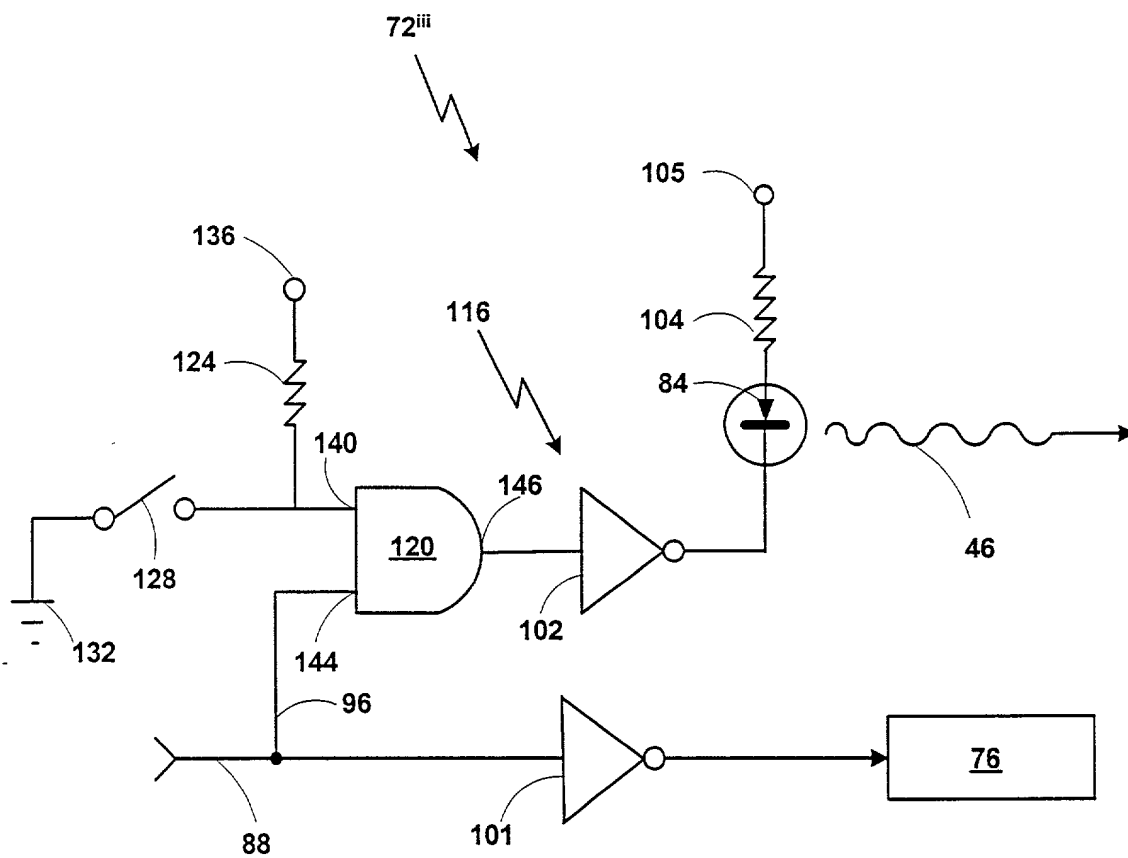


Fig. 7

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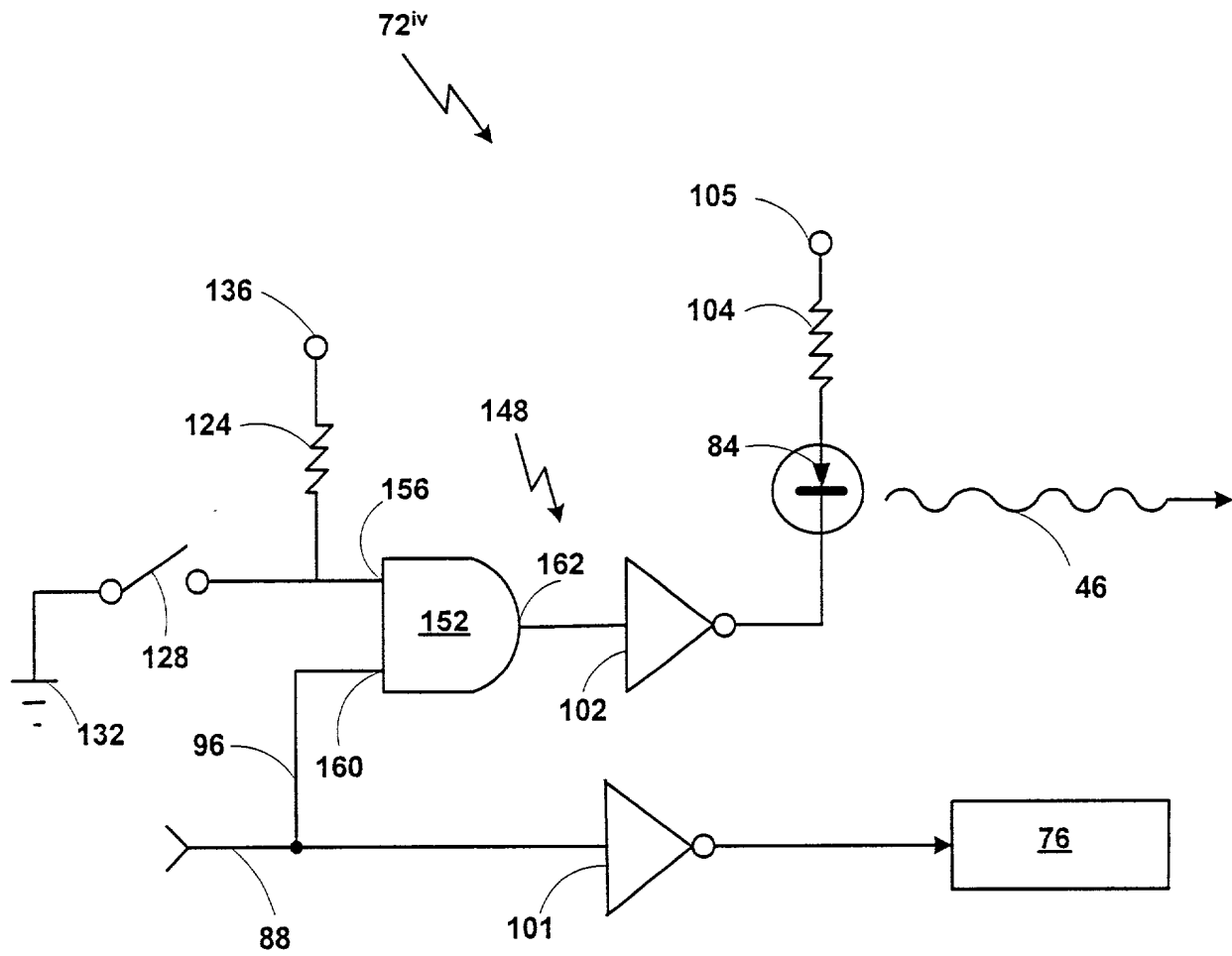


Fig. 8

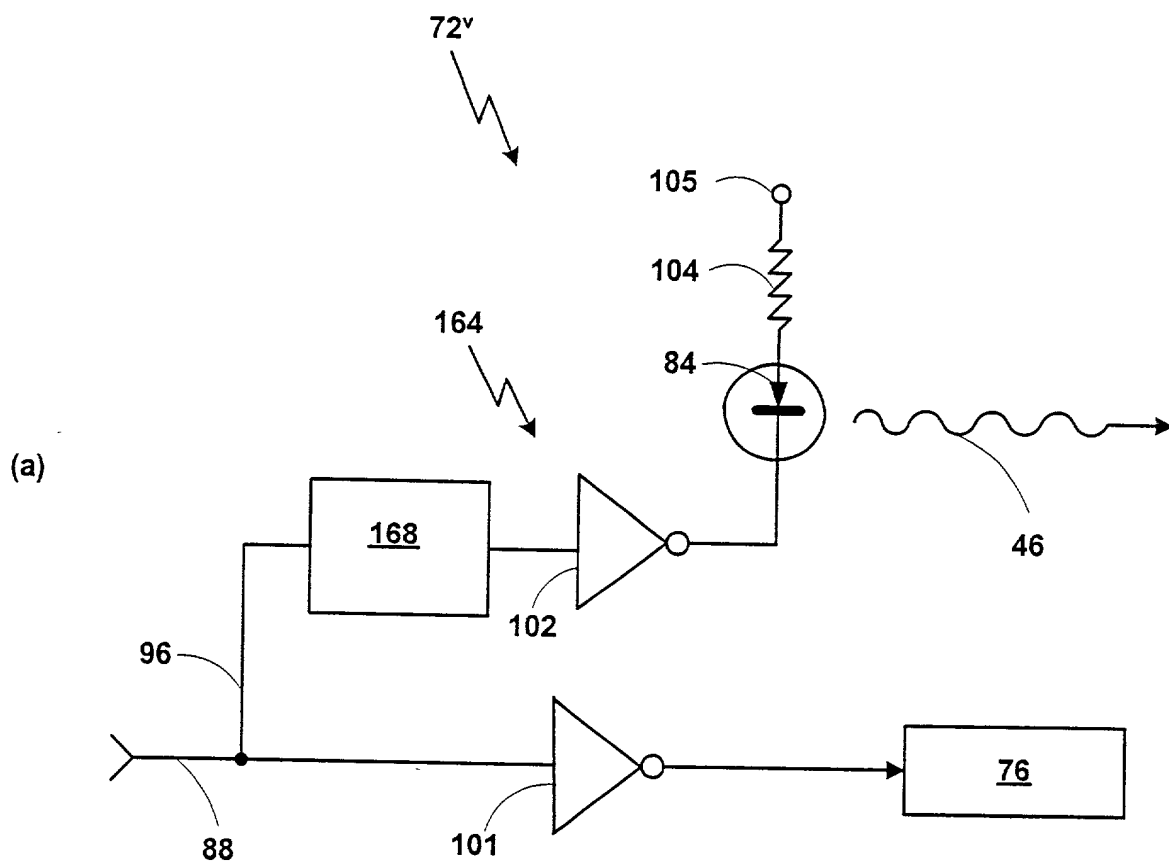


Fig. 9

The diagram illustrates the timing of a three-phase inverter. The top section shows the phase voltages: 200 (reference), 204a, 204b, and 204c. The bottom section shows the switching signals: 212 (output) and 216a, 216b, 216c (switching states). The time axis is marked with t_0, t_1, t_2, t_3 . The duration of the switching cycle is indicated as $1/2 UI$ and UI , with a total duration of 220 .

Fig. 10

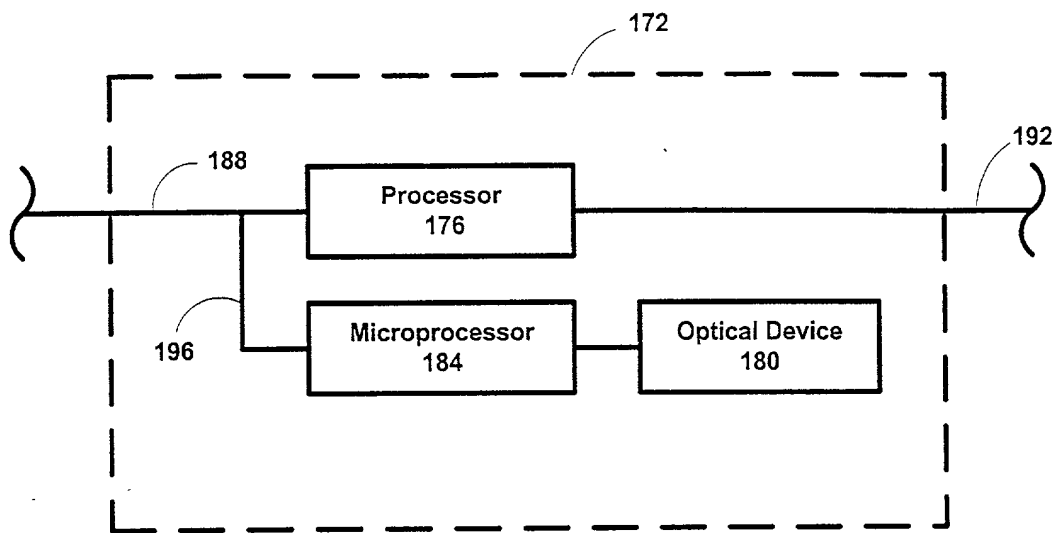


Fig. 11

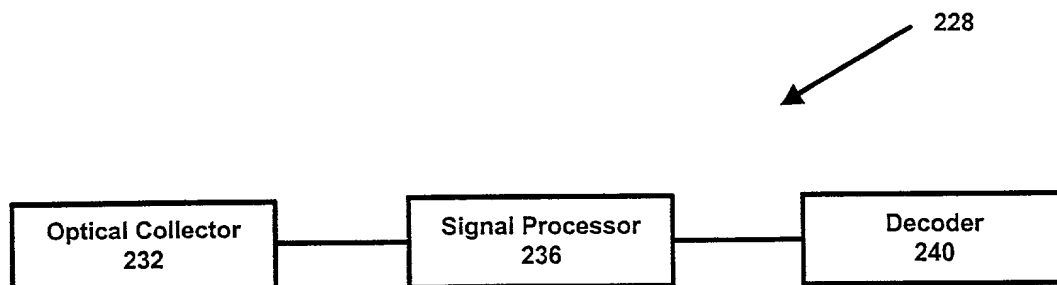


Fig. 12

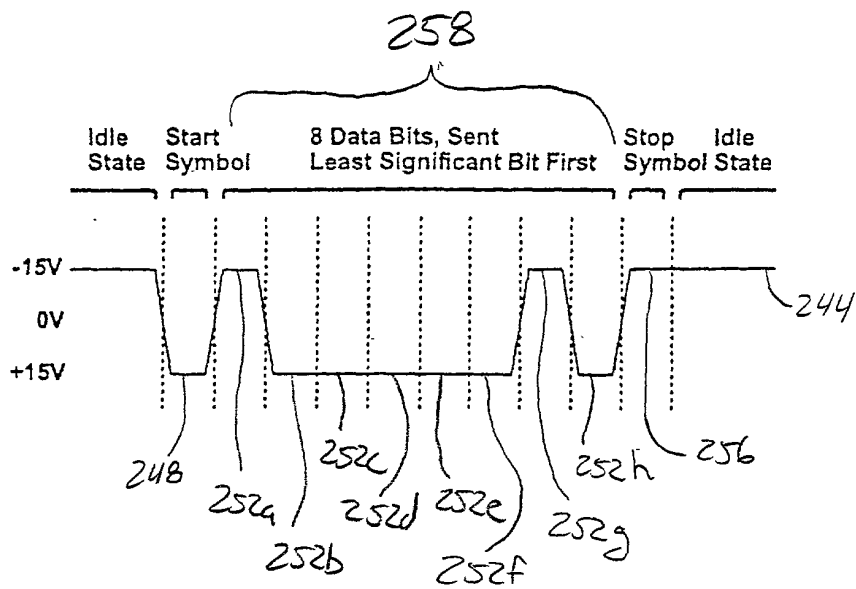


FIG. 13

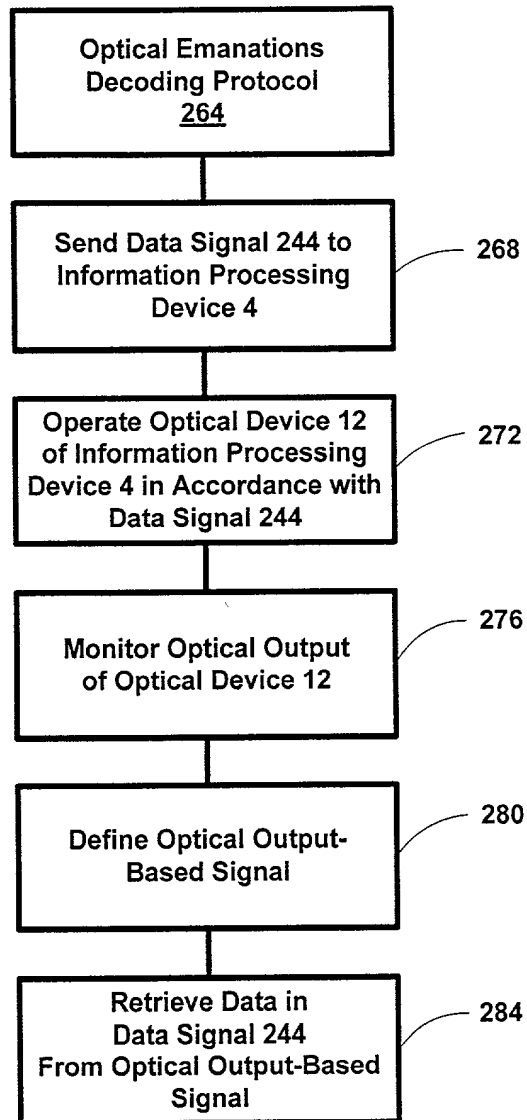


Fig. 14A

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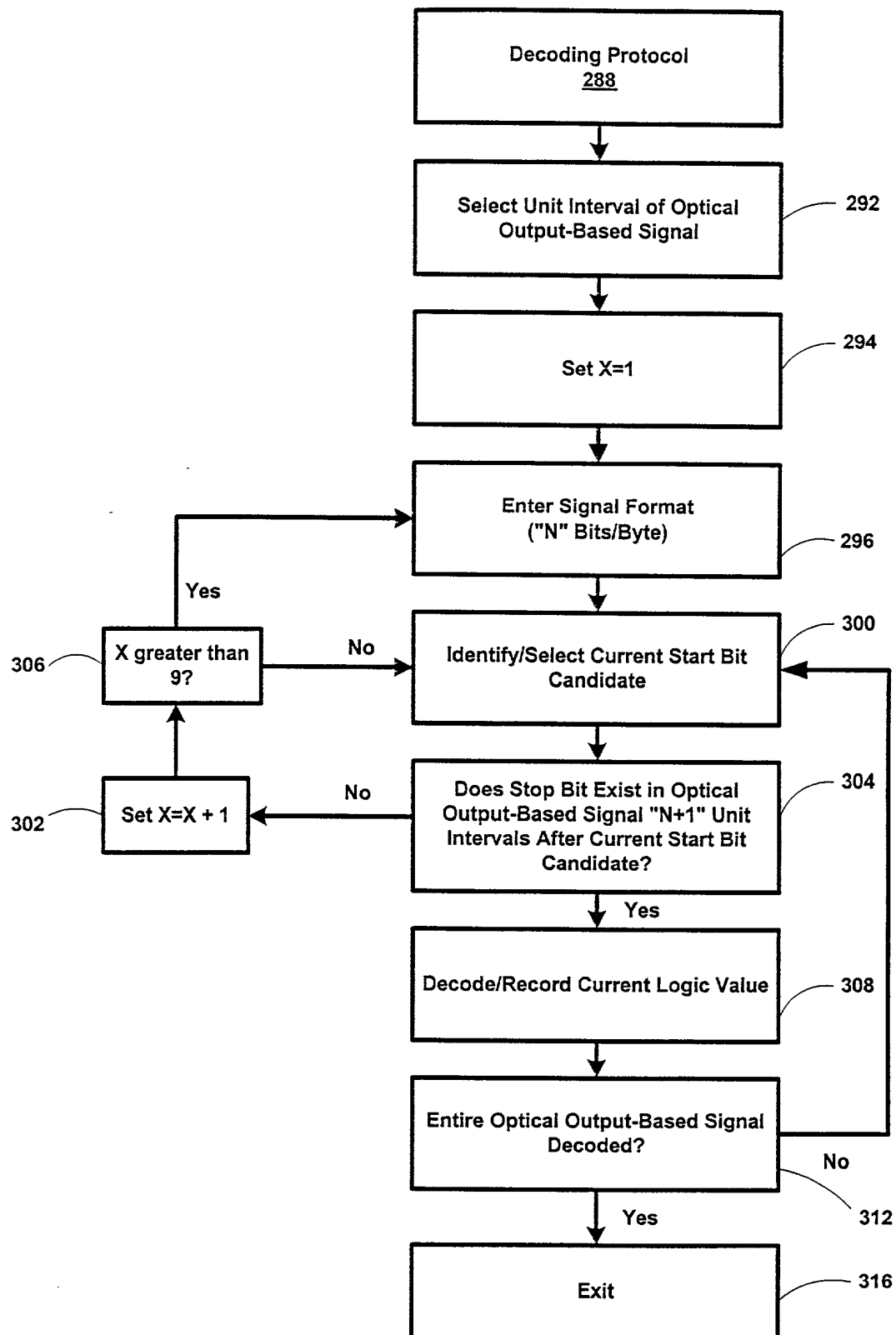


Fig. 14B

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Tek **Stop** Single Seq 50.0kS/s

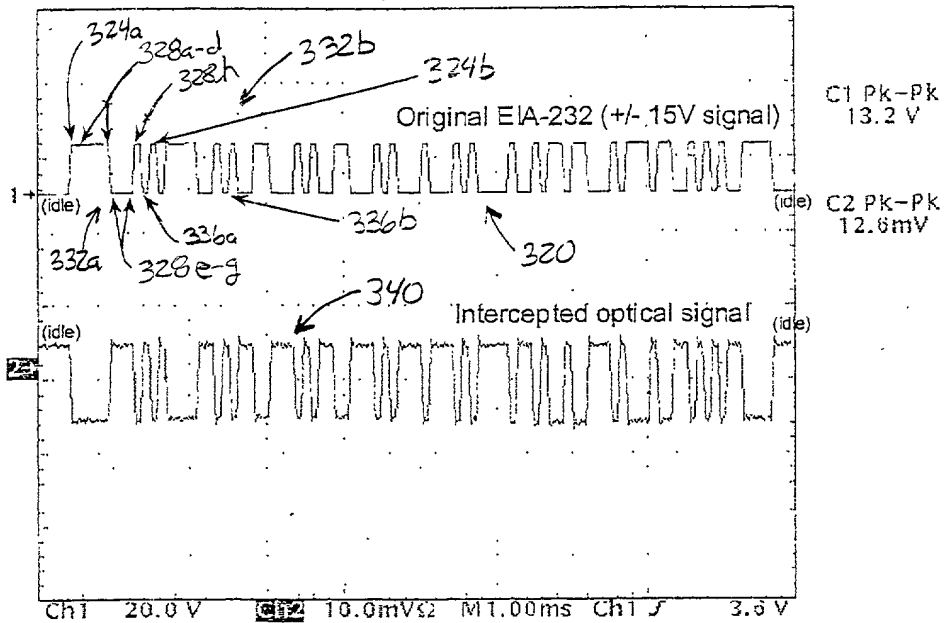


FIG. 15A

Character	In Binary	(reverse the bits)	Reversed and framed by start / stop bits
p	01010000	00001010	0000011101 — 368a
a	01100001	10000110	0100001101 — 368b
s	01110011	11001110	0110011101
s	01110011	11001110	0110011101
w	01110111	11101110	0111011101
o	01101111	11110110	0111101101
r	01110010	01001110	0010011101
d	01100100	00100110	0001001101
<return>	00001011	11010000	0110100001

FIG. 15B

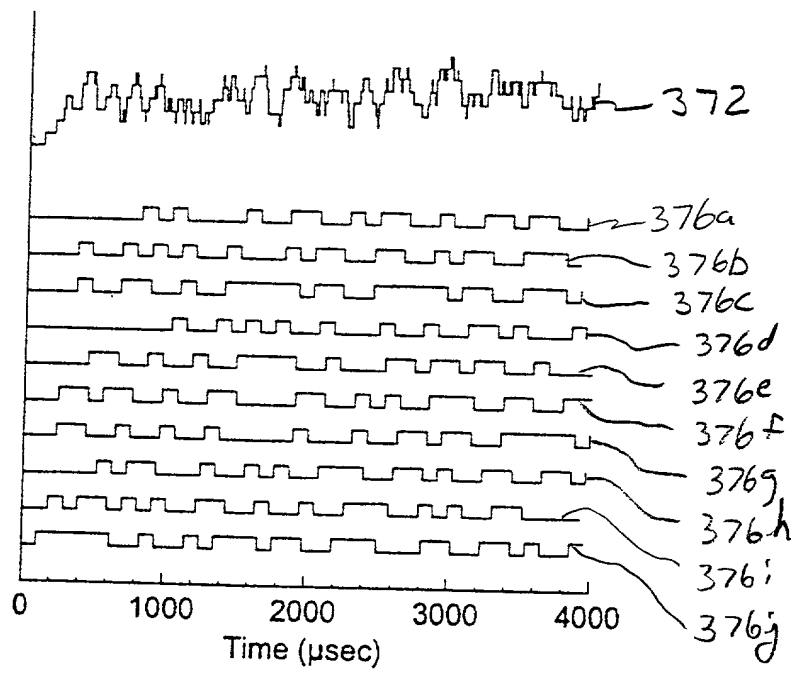


Fig. 16

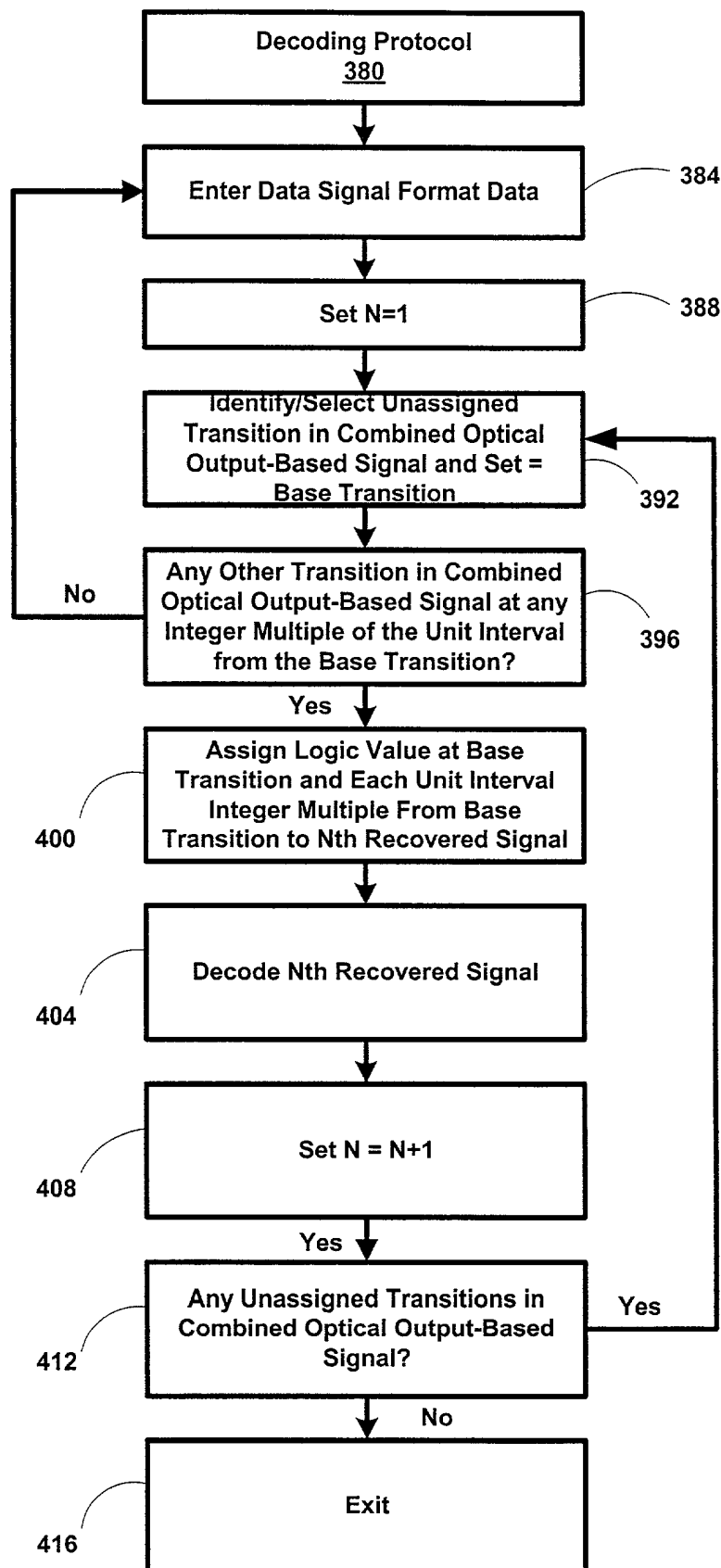


Fig. 17

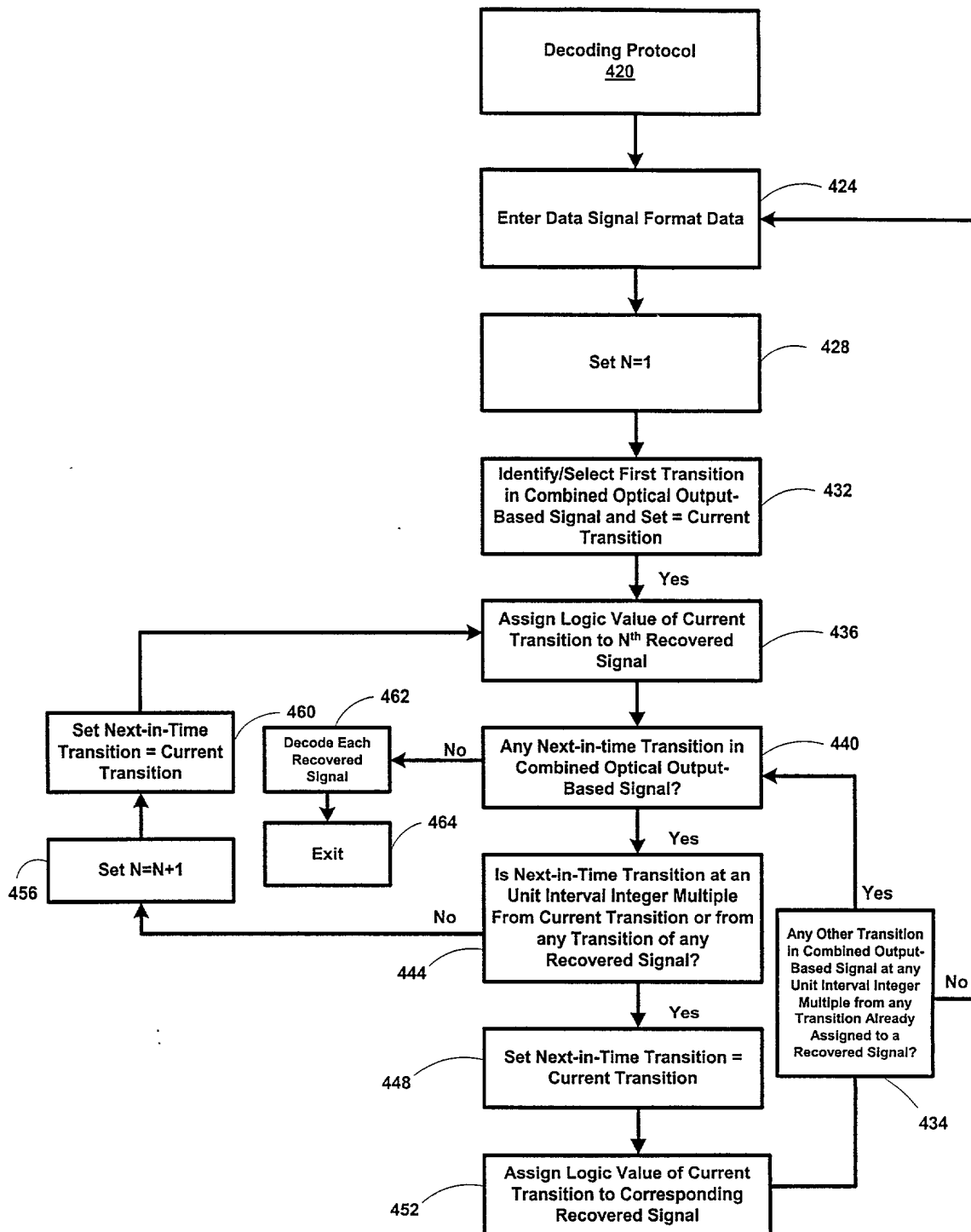


Fig. 18

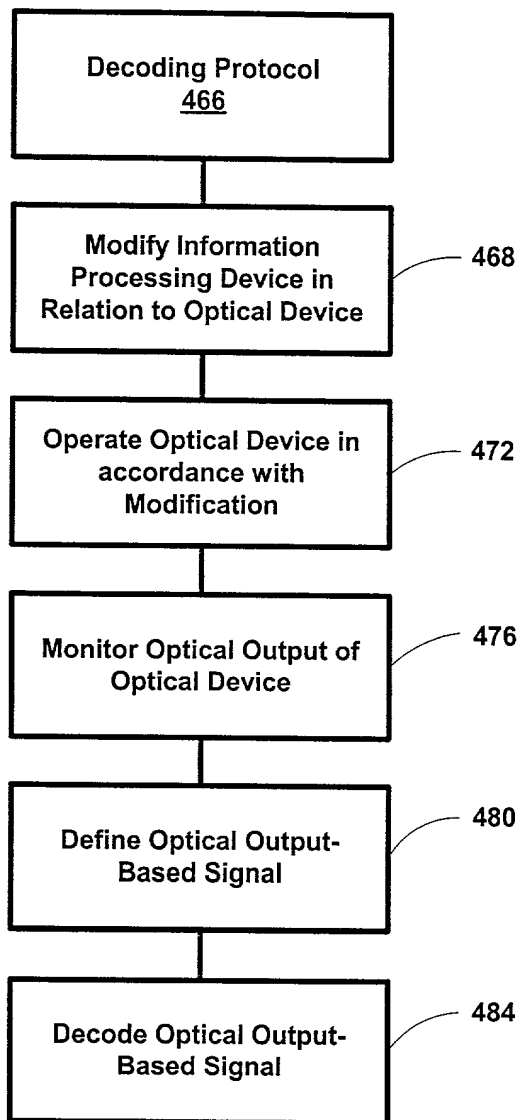


Fig. 19

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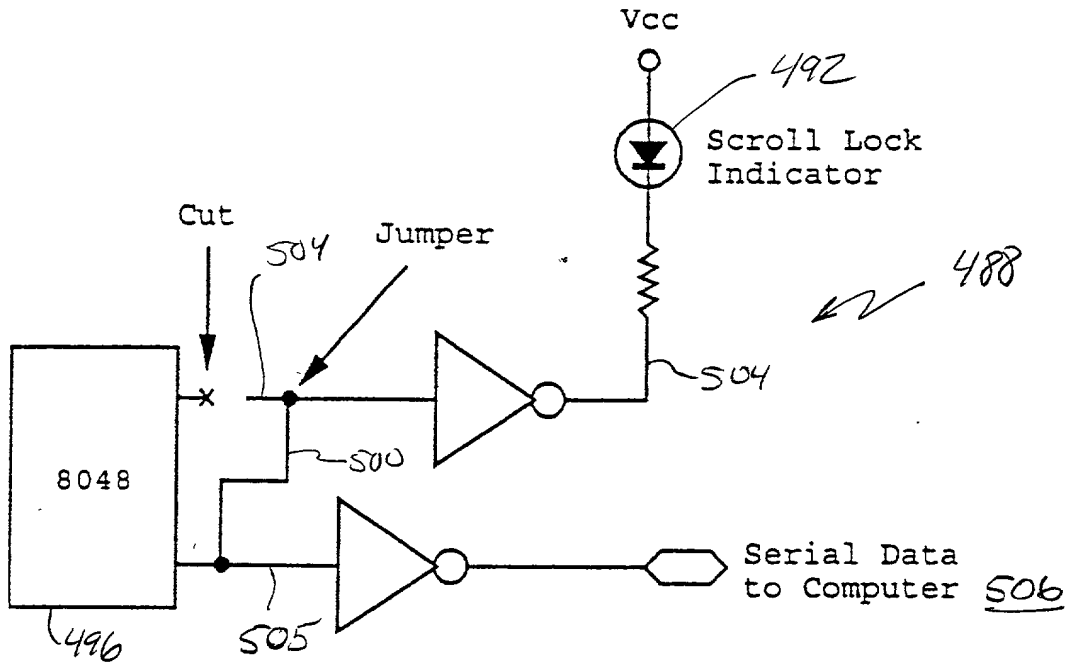


FIG. 20

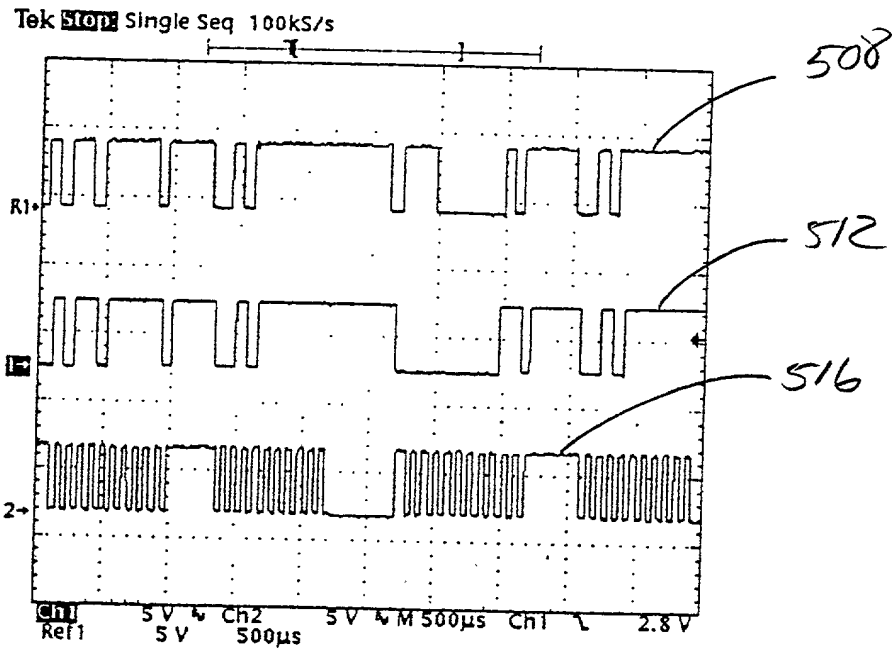


FIG. 21